Claims

The following is a copy of Applicants' claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("——"), as is applicable:

1.   (Currently Amended) A low power voltage-to-current converter for use in a phase locked loop, comprising:

an input stage comprising:

a pair of differential signal input terminals operable to receive differential input signals;

first and second switching transistors each coupled to one of the pair of differential signal input terminals;

first and second complementary transistors coupled to the first and second switching transistor, respectively;

an first output stage and a second output stage, the first output stage coupled to the second output stage, the first output stage coupled to the first complementary transistor of the input stage;

and

a non-differential output terminal coupled to the first output stage, where the output terminal is operable to transmit an output current signal as a function of the differential input signals and independent of a coupled load.

2.   (Previously Presented) The voltage-to-current converter of claim 1, where the input stage is a rail-to-rail input stage.

3.   (Previously Presented) The voltage-to-current converter of claim 2, where the rail-to-rail input stage is a resistorless input stage.

4.   (Currently Amended) The voltage-to-current converter of claim 1, ~~wherein the output stage includes a first output stage and the second output stage,~~ wherein the first output stage and the second output stage each include a constant current source that provides a substantially constant current for the center frequency of the phase lock loop output when the difference between the differential input signals is substantially zero.

5.   (Currently Amended) The voltage-to-current converter of claim 4, wherein the first output stage comprises a first current source transistor<u>, a second current source transistor, a first current sink transistor,</u> and a <u>second</u> current sink transistor, and the second output stage comprises a second <u>stage</u> current source transistor and a ~~second~~ <u>bandgap reference receive</u> transistor.

6.   (Currently Amended) The voltage-to-current converter of claim 5, wherein the ~~second~~ <u>bandgap reference receive</u> transistor of the second output stage is coupled to a bandgap reference signal.

7.   (Previously Presented)   The voltage-to-current converter of claim 6, wherein the bandgap reference signal is approximately 1.23 to 1.25 volts.

8.   (Previously Presented)   The voltage-to-current converter of claim 1, further comprising a biasing transistor coupled to a bias signal coupled to the output of a charge pump of the phase locked loop and to a supply voltage, wherein the biasing transistor is configured to generate a bias current for the first and second complementary transistors of the input stage.

9-15.   (Cancelled)

16.   (Previously Presented) The voltage-to-current converter of claim 8, wherein the bias signal is provided from the supply voltage and a voltage divider circuit of the charge pump.

17.   (Previously Presented) The voltage-to-current converter of claim 1, wherein the differential signal input terminals are coupled to a charge pump circuit and the non-differential output terminal is coupled to a current controlled oscillator.

18.   (Previously Presented) The voltage-to-current converter of claim 17, wherein the charge pump circuit includes a loop filter.